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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,724	06/26/2003	Billy D. Hart	02CR168/KE	5809

7590 10/13/2006

ROCKWELL COLLINS, INC.
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EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

SF

Office Action Summary	Application No.	Applicant(s)	
	10/606,724	HART ET AL.	
	Examiner	Art Unit	
	Kevin M. Burd	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5,7-16,18 and 19* is/are rejected.

7)☒ Claim(s) *6 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the digital quadrature mix for filtering and decimation-by-two must be shown or the feature canceled from the claims. No new matter should be entered. The digital quadrature mix 25 in figure 1 does not show filtering and decimation as stated in claims 1 and 12. Filter and decimate stages 30 shows those functions.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7-16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loseke (US 6,449,244) in view of McLaughlin et al (US 6,442,216) further in view of Schuurmans ((US 7,079,061).

Regarding claims 1 and 4, Loseke discloses an apparatus for efficiently performing parallel processing of high-speed samples comprising an A/D converter 14 in figure 1 (column 6, lines 16-18). Demux 16 is a serial-to-parallel converter for converting the samples from the A/D 14 into parallel samples. Loseke discloses the demultiplexed data outputs 18 are converted from real to complex data representations (column 6, lines 30-32). The real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54). Loseke does not disclose filtering and decimation-by-two the parallel signals. McLaughlin discloses a signal coupled to a cascade of two box car (comb) filters to prevent aliasing before down sampling (column 3, lines 1-4). The down samplers decimate the incoming signal by two (column 3, lines 36-38). McLaughlin states the purpose of the first stage is to reduce the size of the main post detection filter. This is required because the sample rate in the preferred embodiment is much higher than the sampling rate predicted from the bandwidth of the incoming signal (column 3, lines 1-9). For this reason, it would

have been obvious for one of ordinary skill in the art at the time of the invention to combine the filter and decimator of McLaughlin into the apparatus of Loseke. The combination of Loseke and McLaughlin discloses an A/D converter for converting the received analog signal but does not disclose the A/D converter is a 1-bit A/D converter. Schuurmans discloses a sigma delta A/D converter that is a 1-bit A/D converter (column 1, lines 20-35). Schuurmans discloses an advantage of the 1-bit A/D converter is that it has a perfect linearity. In addition the converter is a simple circuit (column 1, lines 20-25) and therefore will reduce the cost and complexity of the circuit. For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the 1-bit A/D converter of Schuurmans into the apparatus of the combination of Loseke and McLaughlin.

Regarding claim 2, McLaughlin discloses the sample rate is 19200 Hz as a result of the decimate stage disclosed above (column 3, lines 61-65).

Regarding claims 3, Loseke discloses the real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54) from the quadrature mix circuit.

Regarding claim 5, McLaughlin discloses a signal coupled to a cascade of two box car (comb) filters to prevent aliasing before down sampling (column 3, lines 1-4). The down samplers decimate the incoming signal by two (column 3, lines 36-38) as stated above.

Regarding claims 7, 10, Loseke discloses a method of implementing an apparatus for efficiently performing parallel processing of high-speed samples

comprising an A/D converter 14 in figure 1 (column 6, lines 16-18). Demux 16 is a serial-to-parallel converter for converting the samples from the A/D 14 into parallel samples. Loseke discloses the demultiplexed data outputs 18 are converted from real to complex data representations (column 6, lines 30-32). The real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54). Loseke does not disclose filtering and decimation-by-two the parallel signals. McLaughlin discloses a signal coupled to a cascade of two box car (comb) filters to prevent aliasing before down sampling (column 3, lines 1-4). The down samplers decimate the incoming signal by two (column 3, lines 36-38). McLaughlin states the purpose of the first stage is to reduce the size of the main post detection filter. This is required because the sample rate in the preferred embodiment is much higher than the sampling rate predicted from the bandwidth of the incoming signal (column 3, lines 1-9). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the filter and decimator of McLaughlin into the apparatus of Loseke. The combination of Loseke and McLaughlin discloses an A/D converter for converting the received analog signal but does not disclose the A/D converter is a 1-bit A/D converter. Schuurmans discloses a sigma delta A/D converter that is a 1-bit A/D converter (column 1, lines 20-35). Schuurmans discloses an advantage of the 1-bit A/D converter is that it has a perfect linearity. In addition the converter is a simple circuit (column 1, lines 20-25) and therefore will reduce the cost and complexity of the circuit. For these reasons, it would have been obvious for one of

ordinary skill in the art at the time of the invention to combine the 1-bit A/D converter of Schuurmans into the apparatus of the combination of Loseke and McLaughlin.

Regarding claim 8, McLaughlin discloses the sample rate is 19200 Hz as a result of the decimate stage disclosed above (column 3, lines 61-65).

Regarding claim 9, Loseke discloses the real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54) from the quadrature mix circuit.

Regarding claim 11, McLaughlin discloses a signal coupled to a cascade of two box car (comb) filters to prevent aliasing before down sampling (column 3, lines 1-4). The down samplers decimate the incoming signal by two (column 3, lines 36-38) as stated above.

Regarding claims 12, 15, 18 and 19, Loseke discloses an apparatus for efficiently performing parallel processing of high-speed samples comprising an A/D converter 14 in figure 1 (column 6, lines 16-18). Demux 16 is a serial-to-parallel converter for converting the samples from the A/D 14 into parallel samples. Loseke discloses the demultiplexed data outputs 18 are converted from real to complex data representations (column 6, lines 30-32). The real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54). Loseke does not disclose filtering and decimation-by-two the parallel signals. McLaughlin discloses a signal coupled to a cascade of two box car (comb) filters to prevent aliasing before down sampling (column 3, lines 1-4). The down samplers decimate the incoming signal by two (column 3, lines 36-38). McLaughlin discloses the sample rate is 19200 Hz as a

result of the decimate stage disclosed above (column 3, lines 61-65). McLaughlin states the purpose of the first stage is to reduce the size of the main post detection filter. This is required because the sample rate in the preferred embodiment is much higher than the sampling rate predicted from the bandwidth of the incoming signal (column 3, lines 1-9). For this reason, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the filter and decimator of McLaughlin into the apparatus of Loseke. The combination of Loseke and McLaughlin discloses an A/D converter for converting the received analog signal but does not disclose the A/D converter is a 1-bit A/D converter. Schuurmans discloses a sigma delta A/D converter that is a 1-bit A/D converter (column 1, lines 20-35). Schuurmans discloses an advantage of the 1-bit A/D converter is that it has a perfect linearity. In addition the converter is a simple circuit (column 1, lines 20-25) and therefore will reduce the cost and complexity of the circuit. For these reasons, it would have been obvious for one of ordinary skill in the art at the time of the invention to combine the 1-bit A/D converter of Schuurmans into the apparatus of the combination of Loseke and McLaughlin.

Regarding claims 13 and 14, Loseke discloses the real and complex data representations of the input signal are channelized on individual channels (column 6, lines 46-54) from the quadrature mix circuit.

Regarding claim 16, McLaughlin discloses a signal coupled to a cascade of two box car (comb) filters to prevent aliasing before down sampling (column 3, lines 1-4). The down samplers decimate the incoming signal by two (column 3, lines 36-38) as stated above.

Allowable Subject Matter

Claims 6 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Friday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kevin M. Burd
10/11/2006

KEVIN BURD
PRIMARY EXAMINER